## REMARKS

Claims 1-4, 7 and 8 are currently pending claims based on the amendment herein:

The Examiner rejected claims 1-4, 7 and 8 under 35 U.S.C. §102(b) as being anticipated by Machida et al. US Patent No. 5,041,897.

The Examiner rejected claims 1, 2 and 4 under 35 U.S.C. §102(b) as being anticipated by Lee et al. (JP 11-54627).

The Examiner rejected claims 1 and 7 under 35 U.S.C. §102(e) as being anticipated by Stamper US Patent No. 6,111,301.

The Examiner rejected claims 2-4 under 35 U.S.C. §103(a) as being unpatentable over Stamper in view of Motsiff et al. US Patent No. 5,731,624.

Applicants respectfully traverse the §102 and §103 rejections with the following arguments.

### 35 U.S.C. §102

Claims 1-4, 7 and 8are rejected under 35 U.S.C. §102(b) as being anticipated by Machida et al. US Patent No. 5,041,897.

The Examiner alleges that " Machida et al. disclose in fig. 1 a semiconductor device comprising a substrate; at least one fuse 12 embedded within an interior portion of the substrate; a continuous etch resistant layer 16 comprising silicon nitride (as in claim 7) having a thickness which falls within the recited range (as in claim 8) over the at least one fuse; and at least one insulative layer 17 above the etch resistant layer, wherein the etch resistant layer has a slower etch rate than that of the at least one insulative layer thereabove. "

As to claim 1 as amended, Applicants respectfully contend that Machida et al. does not anticipate claim 1, because Machida et al. does not teach each and every feature of claim 1. For example, Machida et al. does not teach the features of "a substrate; at least one fuse embedded within an interior portion of the substrate; a continuous etch resistant layer on an **exterior surface** of the substrate, wherein the etch resistant layer is directly over an entire surface the at least one fuse; and at least one insulative layer directly above the etch resistant layer " (emphasis added). Machida does not teach that a fuse embedded within an interior portion of a substrate comprises an etch resistant layer deposited **on an exterior surface** of the substrate and directly over a fuse embedded within an interior portion of the substrate as described by Applicant's claim 1. In contrast, Machida teaches that a fuse located within a substrate is covered with an insulative layer and that the insulative layer is also located **within the substrate**. Therefore, Applicants contend that Machida does not teach the etch resistant layer deposited **on an exterior surface** of the substrate as taught by Applicant's claim 1. Based on the preceding arguments, Applicants respectfully maintain that Machida et al. does not anticipate claim 1, and that claim 1 is in condition for allowance. Since claims 2-4, 7 and 8 depend from claim 1, Applicants contend that claims 2-4, 7 and 8 are likewise in condition for allowance.

Claims 1, 2 and 4 are rejected under 35 U.S.C. §102(b) as being anticipated by Lee et al. (JP 11-54627).

The Examiner alleges that "Lee et al. disclose in fig. 3 a semiconductor device comprising a substrate; at least one fuse 36 embedded within an interior portion of the substrate; a continuous etch resistant layer 40 over the at least one fuse; and at least one insulative layer 41

above the etch resistant layer, wherein the etch resistant layer has a slower etch rate . than that of the at least one insulative layer thereabove ".

As to claim 1 as amended, Applicants respectfully contend that Lee does not anticipate claim 1, because Lee does not teach each and every feature of claim 1. For example, Lee et al. does not teach the features of "a substrate; a substrate; at least one fuse embedded within an interior portion of the substrate; a continuous etch resistant layer on **an exterior surface** of the substrate, wherein the etch resistant layer is directly over **an entire surface the at least one fuse**; and at least one insulative layer directly above the etch resistant layer" (emphasis added). Lee does not teach a fuse embedded within an interior portion surface of a substrate comprises a continuous etch resistant layer is deposited **on the surface of the substrate** and directly over **an entire surface** of a fuse embedded within the surface of the substrate as described by Applicant's claim 1. In contrast, Lee teaches a fuse located within an interlayer insulation film and that **a portion** of the fuse is covered with some sort of material. Lee does not teach that an **entire surface** of a fuse is covered with **etch resistant layer** and that the **continuous** etch resistant layer is deposited **on the surface of the substrate** as described by Applicant's claim 1. Therefore, Applicants contend that Leea does not teach the preceding features of claim 1. Based on the preceding arguments, Applicants respectfully maintain that Lee et al. does not anticipate claim 1, and that claim 1 is in condition for allowance. Since claims 2-4, 7 and 8 depend from claim 1, Applicants contend that claims 2-4, 7 and 8 are likewise in condition for allowance.

Claims 1 and 7 are rejected under 35 U.S.C. §102(e) as being anticipated by Stamper US Patent No. 6,111,301.

The Examiner alleges that "Stamper discloses in fig. 1 a semiconductor device comprising a substrate; at least one fuse 6 embedded within an interior portion of the substrate; a continuous *etch resistant layer 5 comprising silicon nitride (as in claim 7) over the at least one fuse;* and at least one insulative layer 8 above the etch resistant layer, wherein the etch resistant layer has a slower etch rate than that of the at least one insulative layer thereabove. "

Applicants respectfully contend that Stamper does not anticipate claim 1 as amended, because Stamper does not teach each and every feature of claim 1. For example, Stamper does not teach the features of " a substrate; at least one fuse embedded within an interior portion of the substrate; a continuous etch resistant layer on **an exterior surface** of the substrate, wherein the etch resistant layer is directly over **an entire surface the at least one fuse**; and at least one insulative layer directly above the etch resistant layer ". Stamper does not teach that a fuse is embedded within an interior portion of a substrate and that a **continuous** etch resistant layer is deposited **on the surface of the substrate** and directly over **an entire surface** of a fuse embedded within an interior portion of the substrate as described by Applicant's claim 1. In contrast, Stamper teaches a wire 6 located within a copper diffusion barrier 7 within a film 8 and that a film 5 **partially** covers the wire and is only required if the film 8 will not adhere to the wire 6 (see Stamper, col. 2 lines 45-65 and FIG. 1). Additionally, Applicants contend that the Examiner has incorrectly concluded that the wire 6 of Stamper is a fuse when in fact Stamper in col.2 describes a fusible conductor 1 comprising nothing over the surface of the fusible conductor. Lee does not teach that an **entire surface** of a fuse is covered with **etch resistant layer** as described by Applicant's claim 1. Based on the preceding arguments, Applicants respectfully maintain that Stamper does not anticipate claim 1, and that claim 1 is in condition

for allowance. Since claims 2-4, 7 and 8 depend from claim 1, Applicants contend that claims 2-4, 7 and 8 are likewise in condition for allowance.

## CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims 1-4, 7 and 8 and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below.

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